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Application No. <u>10021676</u>	Prepared by <u>BS</u>	Tracking Number <u>X</u>	
Examiner-GAU <u>SIEK-2825</u>	Date <u>5-3-07</u>	Week Date <u>AS</u>	
	No. of queries <u>1</u>		

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	<u>Other</u>

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1/28/04

24319 7590 12/23/2003
LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106 LEGAL
MILPITAS, CA 95035

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,696	10/30/2001	Michael Eneboe	01-490	9160

TITLE OF INVENTION: SYSTEM AND METHOD FOR OPTIMIZING AN INTEGRATED CIRCUIT DESIGN

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$0	\$1330	03/23/2004
EXAMINER	ART UNIT	CLASS-SUBCLASS			
SIEK, VUTHE	2825	716-002000			

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LSI Logic Corporation

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Leo Peters

33,562

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1/28/04

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